



Ckingway

SPECIFICATION

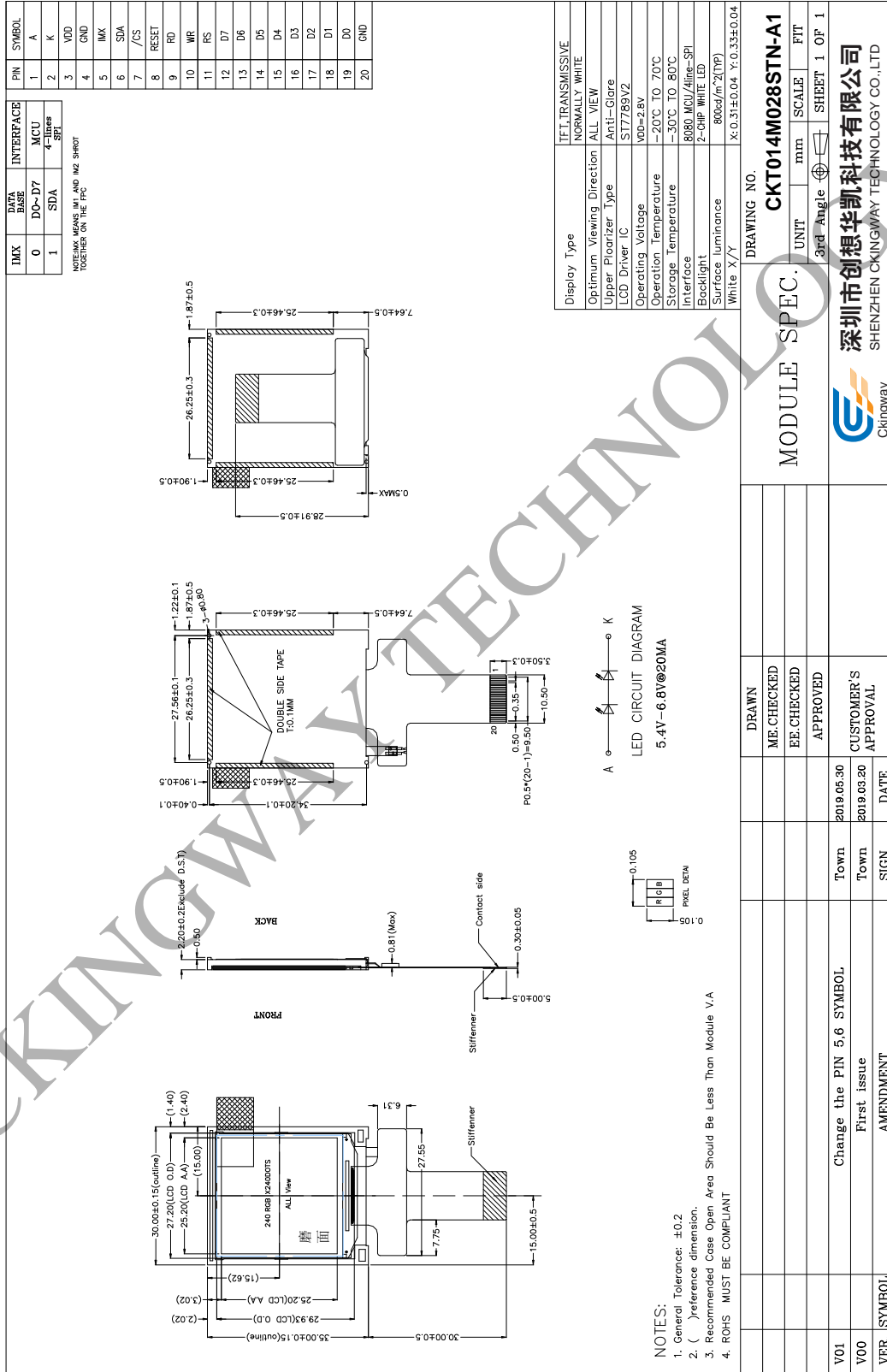
LCD Number: CKT014M028STN-A1

| | | | |
|----------------------|------------|----------|-------------|
| CUSTOMER APPROVED | PREPARE BY | CHECK BY | APPROVED BY |
| | | | |
| | | | |
| SUPPLIER APPROVED | PREPARE BY | CHECK BY | APPROVED BY |
| | | | |

1. General Specification

| Item | Contents | Unit |
|--------------------------------|--------------------|---------|
| LCD TYPE | TFT/TRANSMISSIVE | |
| MODULE SIZE (W*H*T) | 30.00*35.00*2.20 | MM |
| ACTIVE SIZE (W*H) | 25.20*25.20 | MM |
| PIXEL PITCH (W*H) | 0.105*0.105 | MM |
| NUMBER OF DOTS | 240*240 | |
| DRIVER IC | ST7789V2 | |
| INTERFACE TYPE | 8080 MCU/4line-SPI | |
| TOP POLARIZER TYPE | ANTI-GLARE | |
| RECOMMEND VIEWING DIRECTION | ALL | O'CLOCK |
| GRAY SCALE INVERSION DIRECTION | - | O'CLOCK |
| BACKLIGHT TYPE | 2-DIES WHITE LED | |
| TOUCH PANEL TYPE | WITHOUT | |

2. Mechanical Drawing



3. Interface Pin Function

| Pin No. | Symbol | Description | | | | | | | | | |
|--|--------|--|-----------|-----------|-----------|---|-------|-----|---|-----|-------------|
| 1 | LEDA | Anode of LED backlight. | | | | | | | | | |
| 2 | LEDK | Cathode of LED backlight. | | | | | | | | | |
| 3 | VDD | Power supply | | | | | | | | | |
| 4 | GND | Power ground | | | | | | | | | |
| 5 | IMX | <table border="1"> <thead> <tr> <th>IMX</th> <th>DATA BASE</th> <th>INTERFACE</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>D0~D7</td> <td>MCU</td> </tr> <tr> <td>1</td> <td>SDA</td> <td>4-lines SPI</td> </tr> </tbody> </table> | IMX | DATA BASE | INTERFACE | 0 | D0~D7 | MCU | 1 | SDA | 4-lines SPI |
| | | IMX | DATA BASE | INTERFACE | | | | | | | |
| | | 0 | D0~D7 | MCU | | | | | | | |
| 1 | SDA | 4-lines SPI | | | | | | | | | |
| NOTE:IMX MEANS IM1 AND IM2 SHROT TOGETHER ON THE FPC | | | | | | | | | | | |
| 6 | SDA | <p>When IM3: Low, SPI interface input/output pin. When IM3: High, SPI interface input pin. The data is latched on the rising edge of the SCL signal. If not used, please fix this pin at VDDI or DGND level.</p> | | | | | | | | | |
| 7 | /CS | <p>Chip selection pin Low enable. High disable.</p> | | | | | | | | | |
| 8 | RESET | <p>This signal will reset the device and it must be applied to properly initialize the chip. Signal is active low.</p> | | | | | | | | | |
| 9 | RD | <p>Read enable in 8080 MCU parallel interface. If not used, please fix this pin at VDDI or DGND.</p> | | | | | | | | | |
| 10 | WR | <p>Write enable in MCU parallel interface. Display data/command selection pin in 4-line serial interface. Second Data lane in 2 data lane serial interface. If not used, please fix this pin at VDDI or DGND.</p> | | | | | | | | | |
| 11 | RS | <p>A register select signal. Low: select an index or status register, High: select a control register.</p> | | | | | | | | | |
| 12 | D7 | Data bus. | | | | | | | | | |
| 13 | D6 | Data bus. | | | | | | | | | |
| 14 | D5 | Data bus. | | | | | | | | | |
| 15 | D4 | Data bus. | | | | | | | | | |
| 16 | D3 | Data bus. | | | | | | | | | |
| 17 | D2 | Data bus. | | | | | | | | | |
| 18 | D1 | Data bus. | | | | | | | | | |
| 19 | D0 | Data bus. | | | | | | | | | |
| 20 | GND | Power ground. | | | | | | | | | |